T.C.

BİLECİK ŞEYH EDEBALİ ÜNİVERSİTESİ

MÜHENDİSLİK FAKÜLTESİ

ELEKTRİK-ELEKTRONİK MÜHENDİSLİĞİ BÖLÜMÜ

2018-2019 BAHAR DÖNEMİ

EEM432 GÖMÜLÜ SİSTEMLER

DERS NOTU

Arş. Gör. Zeynep KAYA


terasIC
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ALTERA
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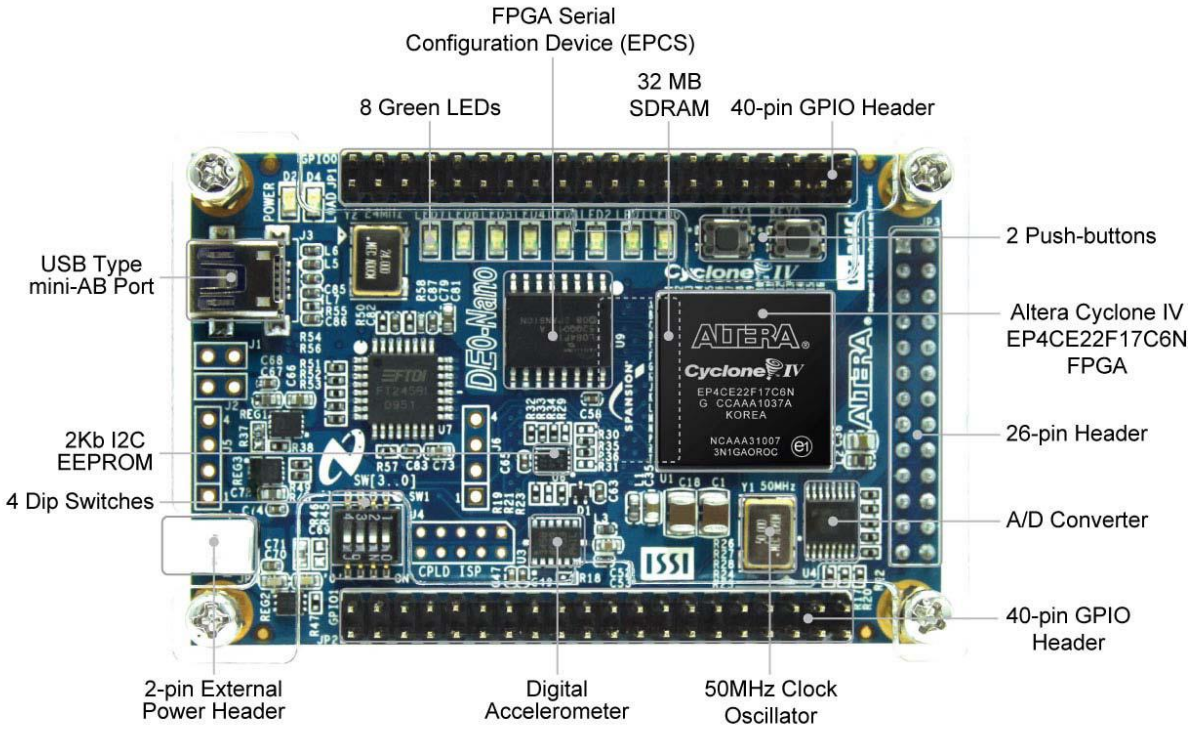
İÇİNDEKİLER **SAYFA**

Altera Cyclone® IV EP4CE22F17C6N FPGA Genel özellikleri

- 153 maximum FPGA I/O pins
- 2 Adet 40 pin grubu (GPIO)
- 32MB SDRAM
- 2KB I2C EEPROM
- 8 Adet Yeşil LED
- 4 Adet Dipswitch
- 2 Adet Push Button
- G Sensörü
- ADC Modülü
- 50 Mhz Osilatör



Cyclone® IV EP4CE22F17C6N Bileşenleri

Kurulum:

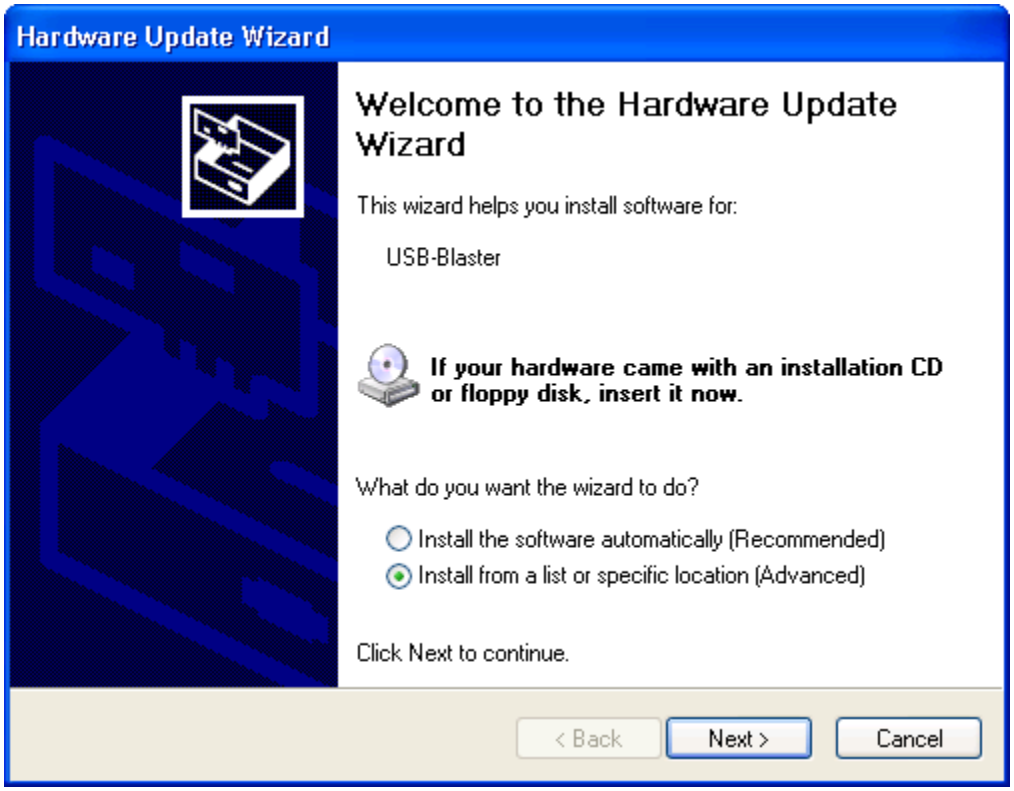
Altera Cyclone® IV EP4CE22F17C6N FPGA Paket İçeriği

❶ Altera DE0-Nano Board
❷ USB Mini-B Cable
❸ DE0-Nano System CD
❹ Altera Complete Design Suite Free Package
❺ DE0-Nano Quick Start Guide

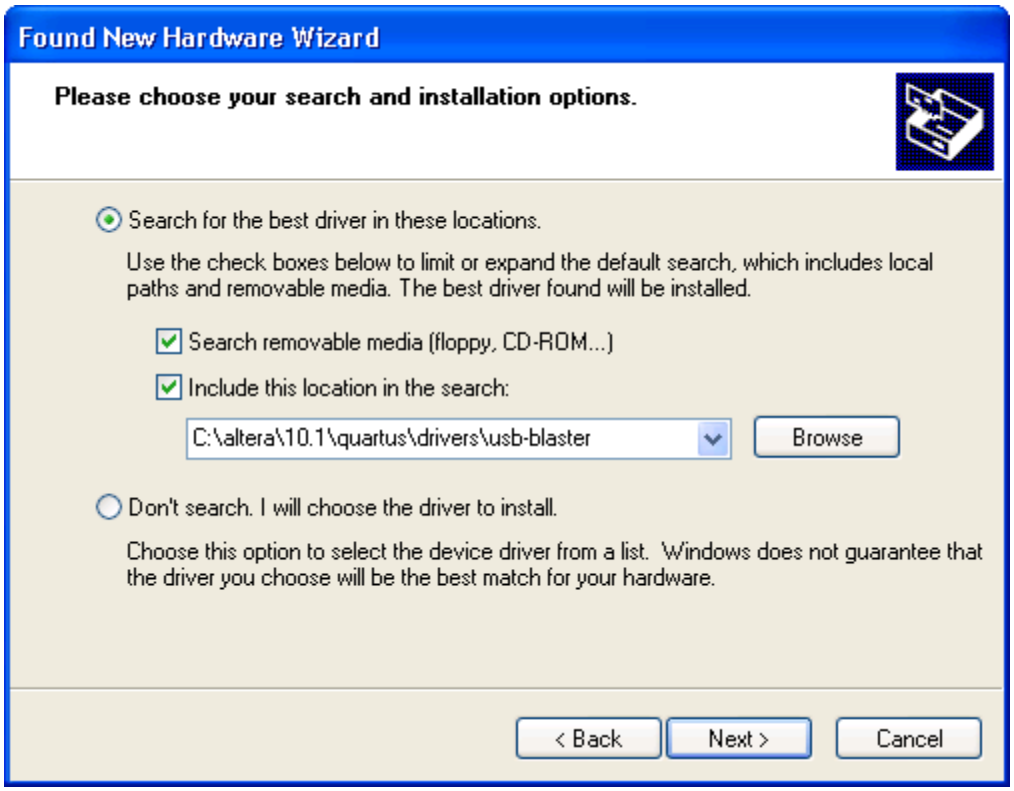
Kurulum CD takıp gerekli kurulum işlemleri yapıldıktan sonra FPGA'yı Bilgisayara tanıtıyoruz bunun için gerekli işlemler aşağıdaki resimlerde gösterilmektedir.

İnternet kurulumu:

https://www.intel.com/content/www/us/en/programmable/downloads/software/quartus-ii-se/101.html#tabs-4



Burada yükleyeceğimiz "USB-BLASTER" dosyasının adresini manuel olarak göstermemiz gerekiyor. Yukarıdaki pencereye "NEXT-İLERİ" diyerek devam ediyoruz.



Burada “BROWSE”Sekmesinden “USB-BLASTER” adresini buluyoruz.

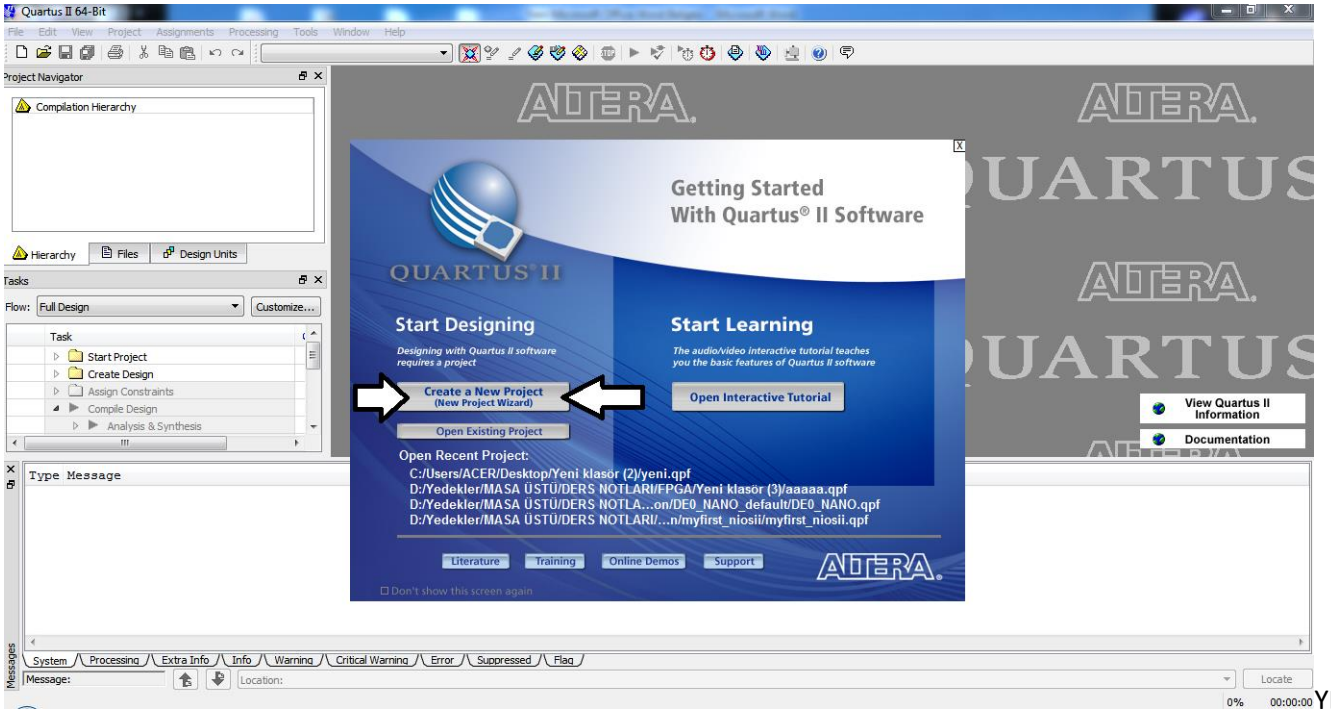
---Aksi durum seçilmediği sürece driver adresi “C:\altera\10.1\quartus\drivers\usb-blaster”

Hedef dosyayı seçip “NEXT-İLERİ”diyoruz.Gelen pencerede yüklemeye devam et diyerek donanım kurulumunu bitiyoruz.

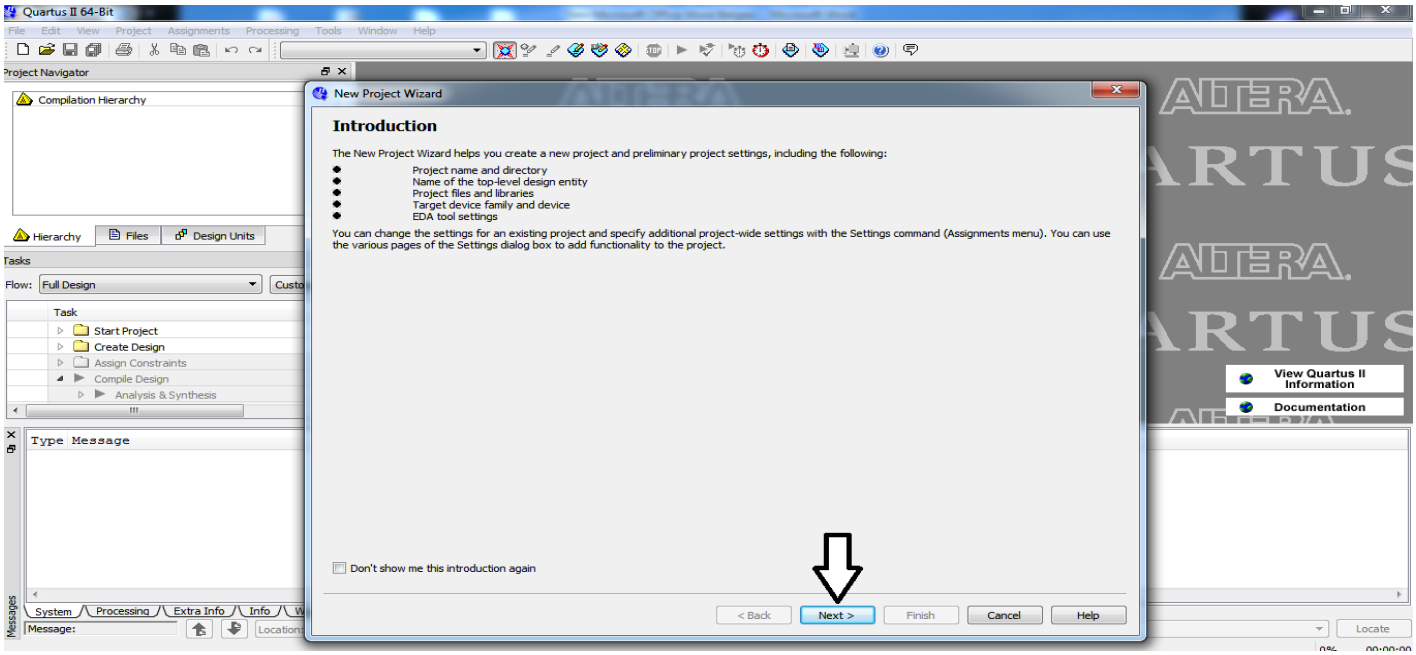
PROGRAMIN ÇALIŞTIRILMASI:

1-Yeni proje oluşturmak

--OK İşaretlerini takip edin!!!

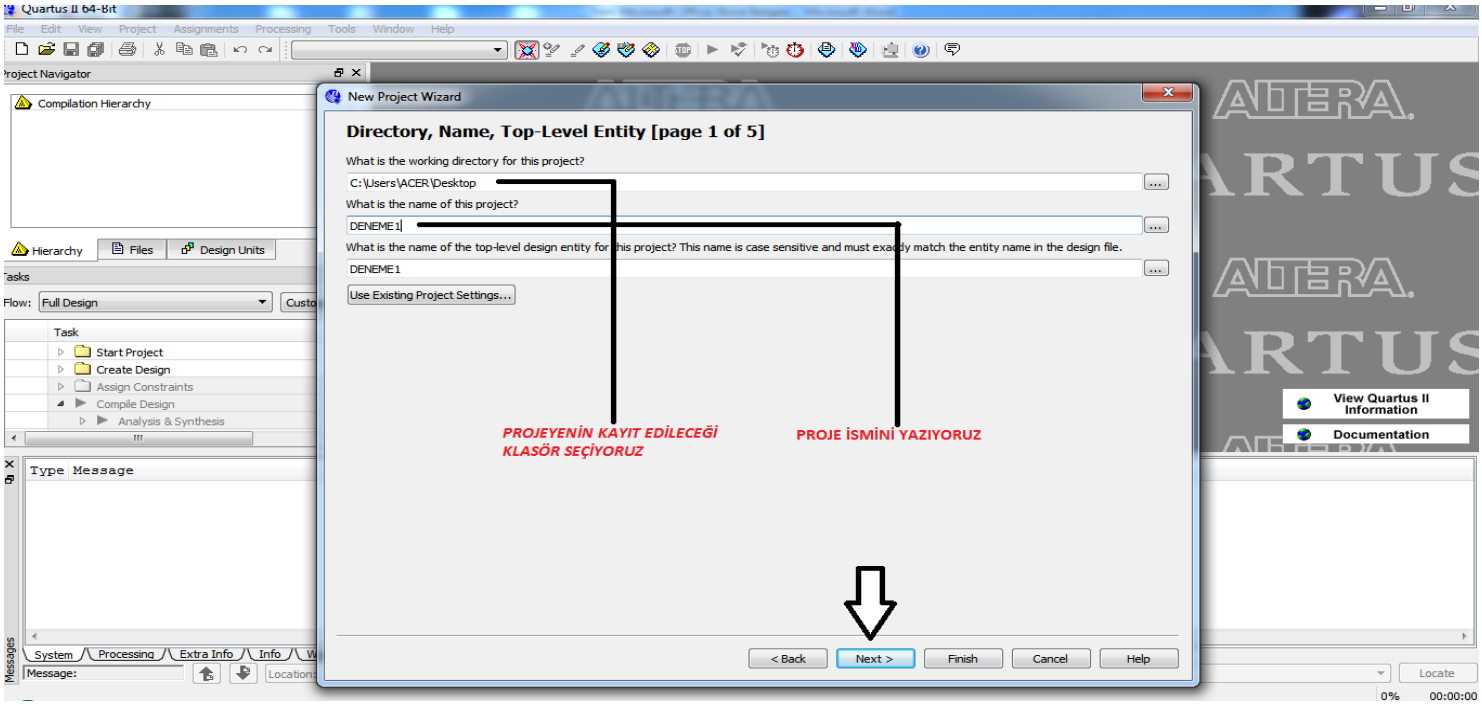


YENİ

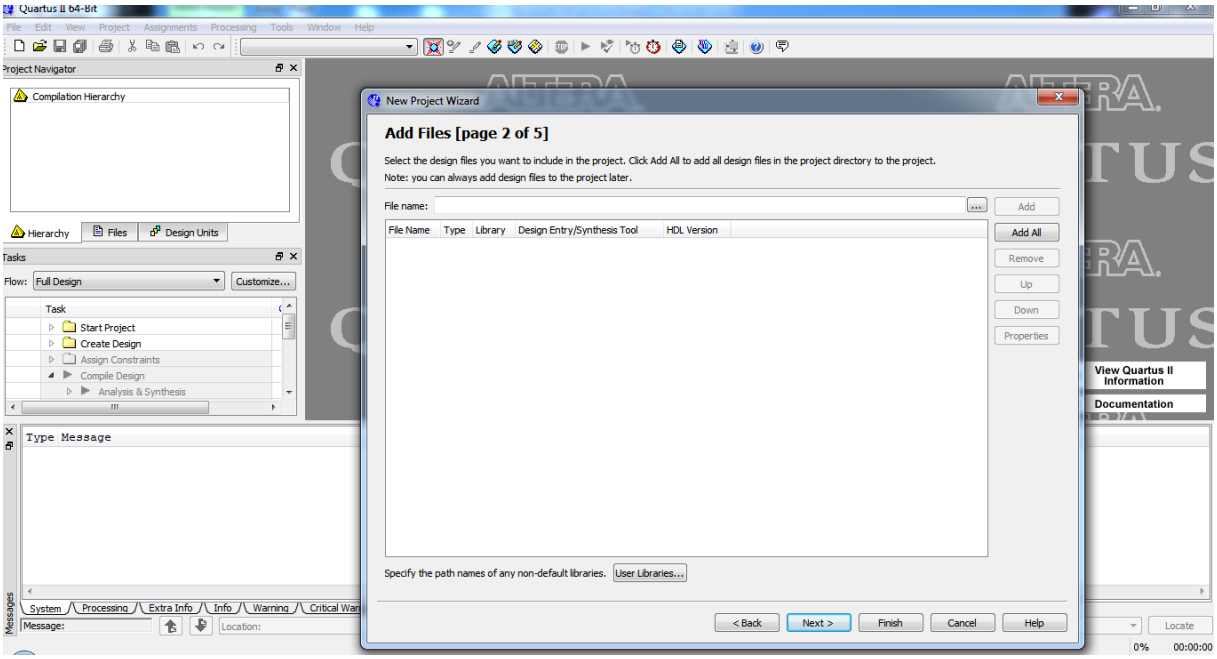


PROJE OLUŞTURUYORUZ

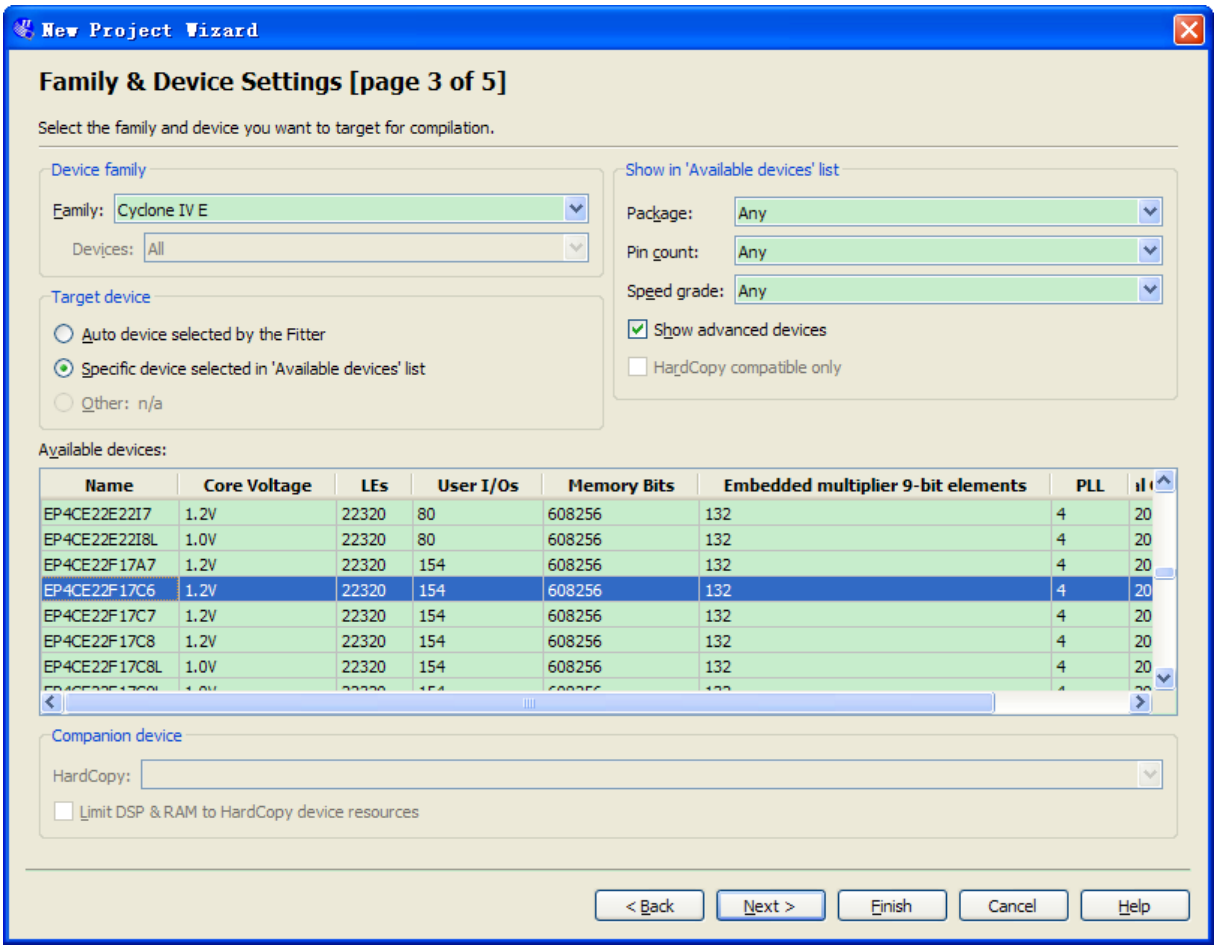
ÇIKAN PENCEREDE “NEXT” Diyerek devam ediyoruz



İşlemlerden sonra “NEXT” diyerek devam ediyoruz

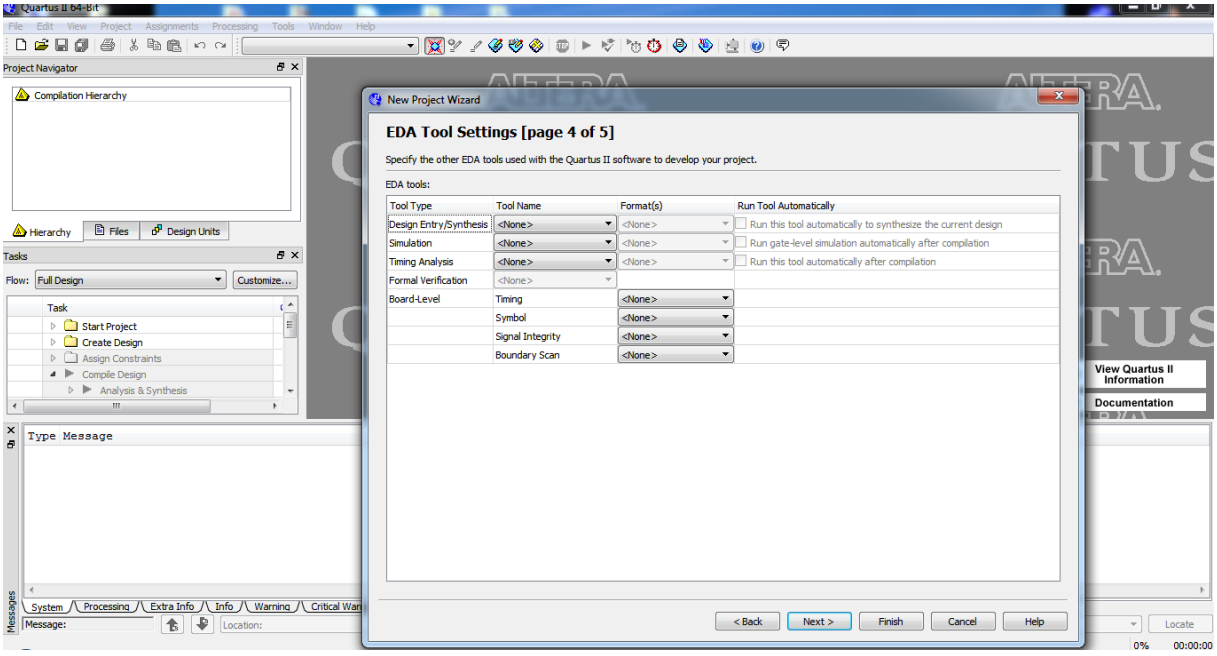


Hiçbir işlem yapmadan “NEXT” Diyerek devam ediyoruz.

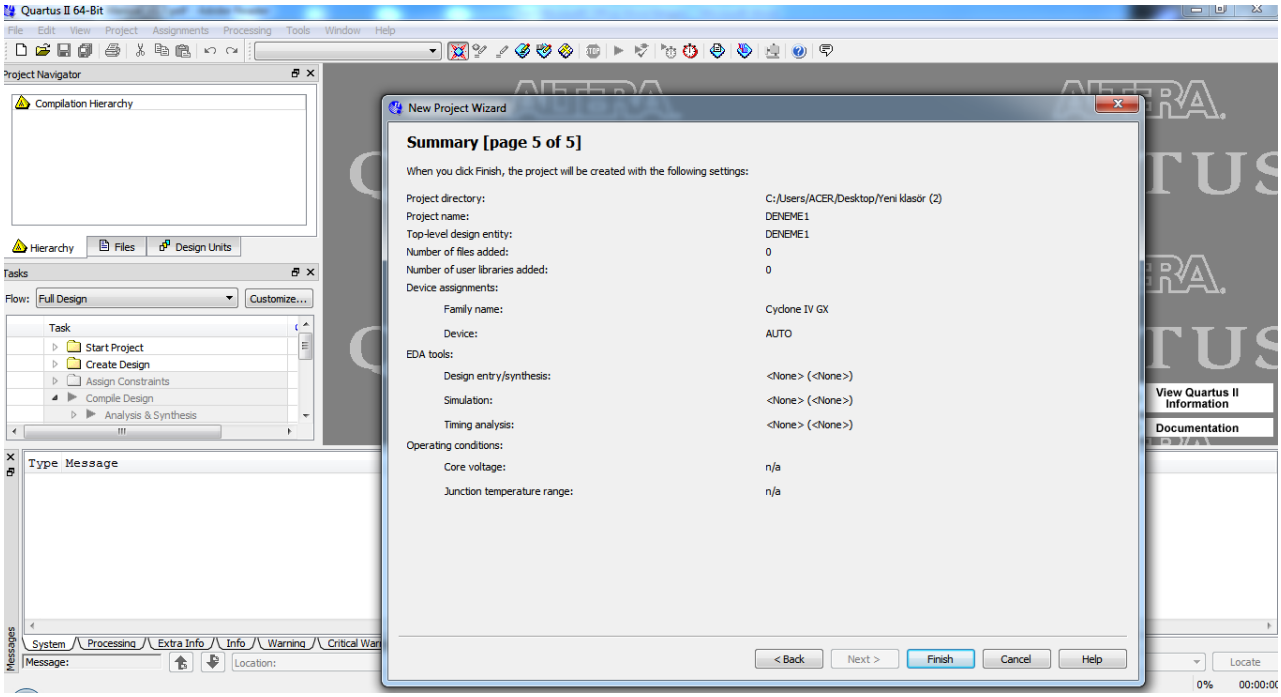


“Altera Cyclone® IV EP4CE22F17C6N” Seçiyoruz ve “NEXT” Diyerek devam ediyoruz

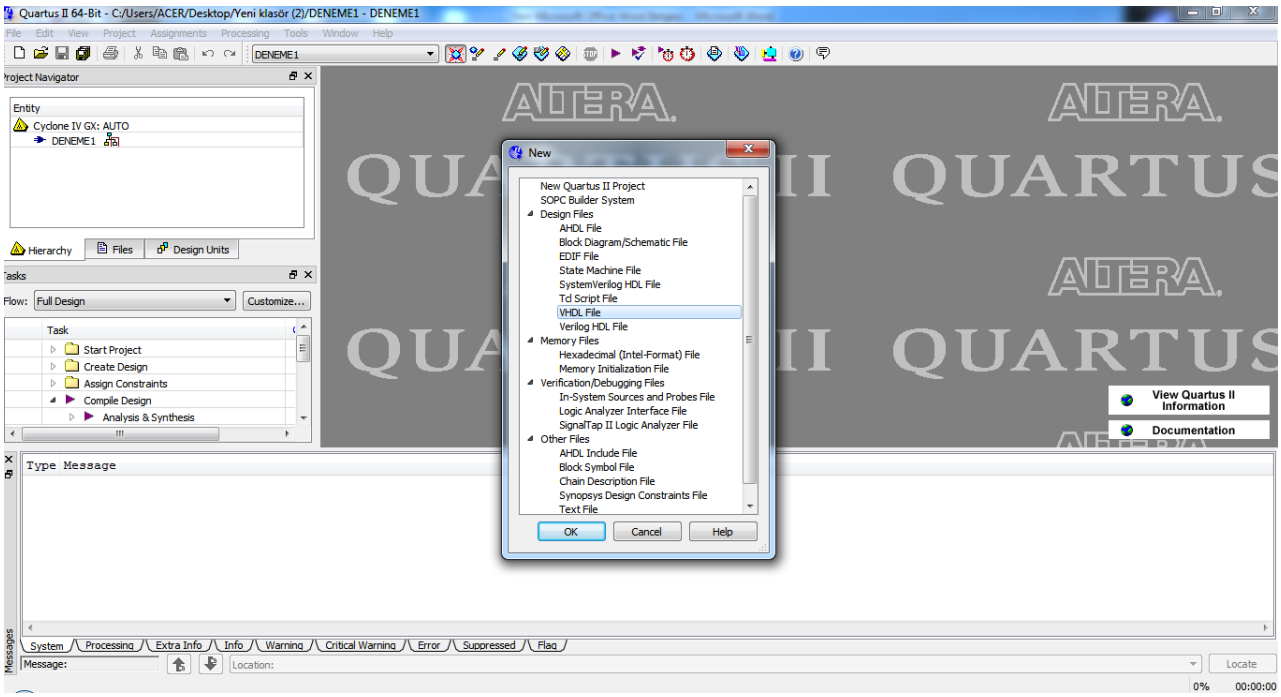
NOT:Başka cihaz seçiminde programınız çalışmaz!!!



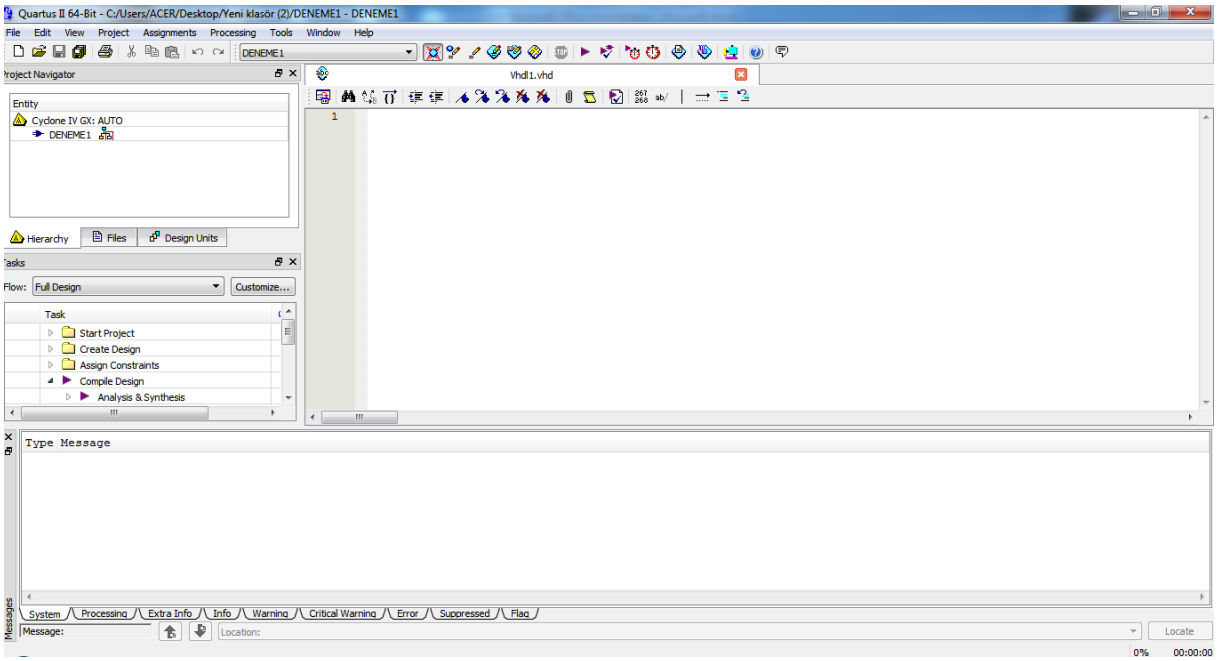
Hiçbir işlem yapmadan”NEXT” Diyerek devam ediyoruz



"FİNİSH" Diyerek kurulumu bitiriyoruz



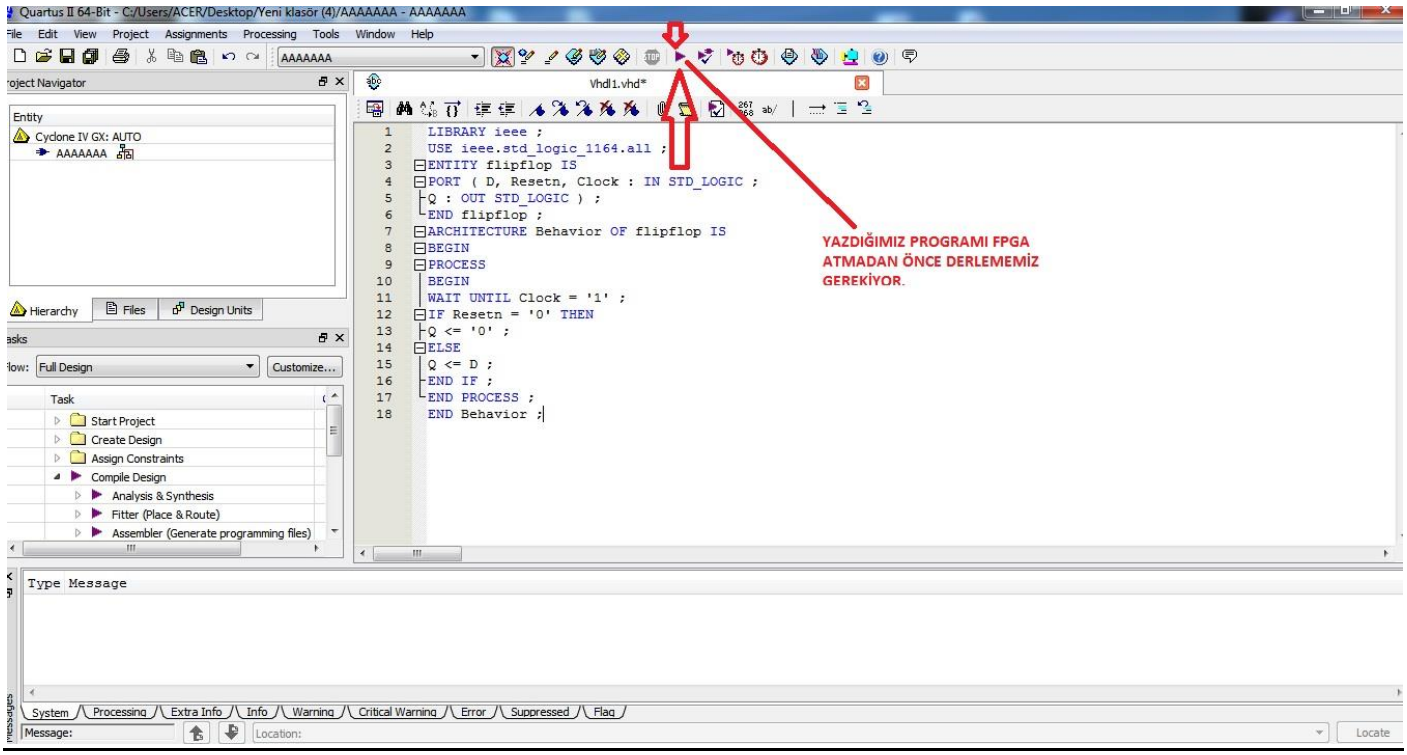
"FİLE-NEW-VHDL FİLE" Seçerek **"OK"** diyoruz



Program yazılmaya hazır örnek VHDL dosyası

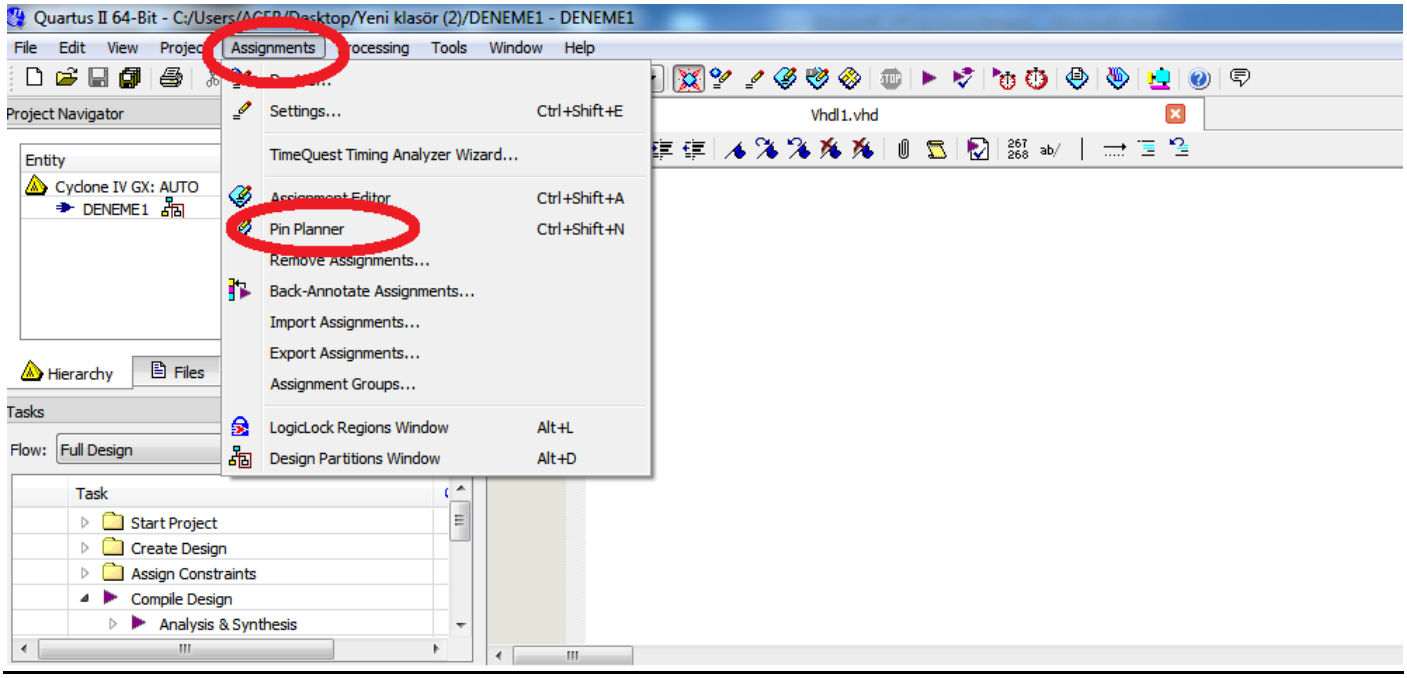
VHDL YAZILIMININ DERLENMESİ:

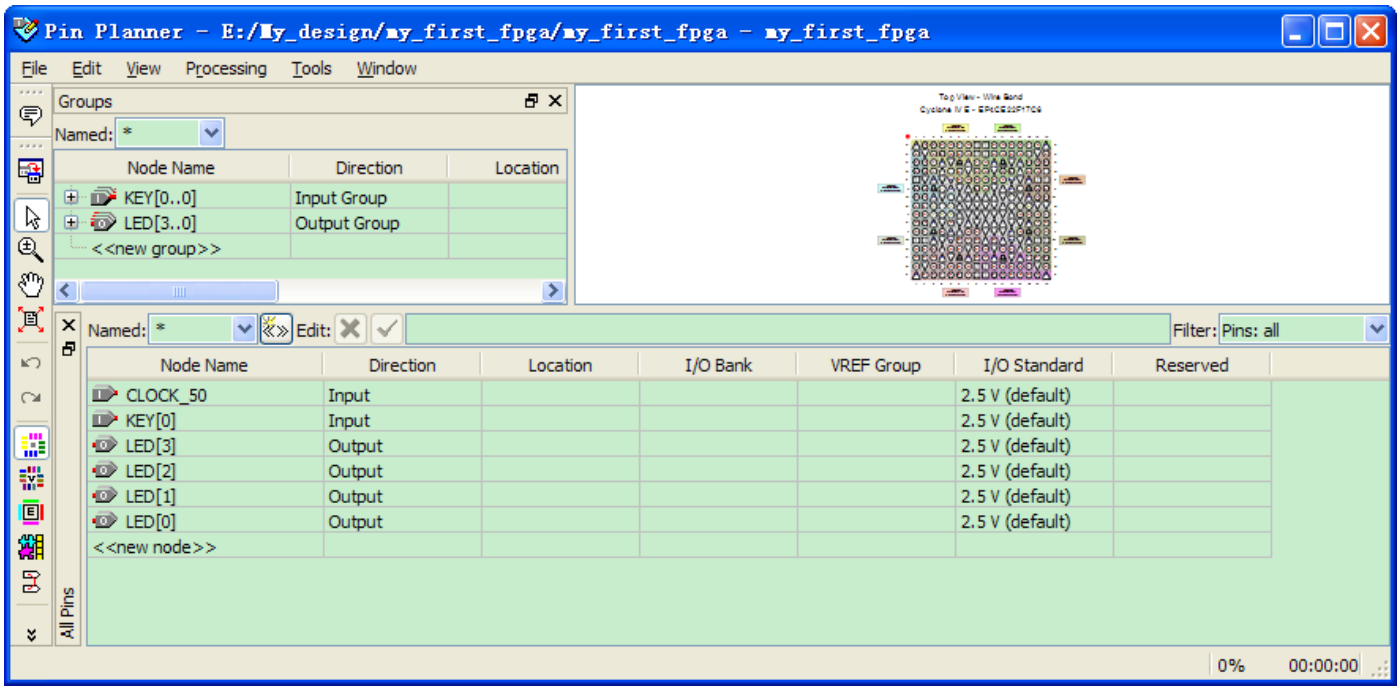
Yazdığımız programın makine diline çevirmemiz için, FPGA yükleme yapmadan önce programımızı Şekilde imgeye basarak “DERLEME” İşlemini gerçekleştiriyoruz. Bu işlemden sonra gerekli error ve hata mesajlarını düzelttikten sonra artık programımızı FPGA atabilir ve deneyebiliriz.



FPGA PİN ATAMALARI:

“Assigments”sekmesinden **“Pin Planner”**seçiyoruz





Aşağıda **“LOCATİON”** sekmesinde yönlendireceğiniz pinlerin numaları bulunmakta.

Signal Name	FPGA Pin No.	Description	I/O Standard
KEY[0]	PIN_J15	Push-button[0]	3.3V
KEY[1]	PIN_E1	Push-button[1]	3.3V

Pusbutton Pinleri

Signal Name	FPGA Pin No.	Description	I/O Standard
LED[0]	PIN_A15	LED Green[0]	3.3V
LED[1]	PIN_A13	LED Green[1]	3.3V
LED[2]	PIN_B13	LED Green[2]	3.3V
LED[3]	PIN_A11	LED Green[3]	3.3V
LED[4]	PIN_D1	LED Green[4]	3.3V
LED[5]	PIN_F3	LED Green[5]	3.3V
LED[6]	PIN_B1	LED Green[6]	3.3V
LED[7]	PIN_L3	LED Green[7]	3.3V

LED Pinleri

Signal Name	FPGA Pin No.	Description	I/O Standard
DIP Switch[0]	PIN_M1	DIP Switch[0]	3.3V
DIP Switch[1]	PIN_T8	DIP Switch[1]	3.3V
DIP Switch[2]	PIN_B9	DIP Switch[2]	3.3V
DIP Switch[3]	PIN_M15	DIP Switch[3]	3.3V

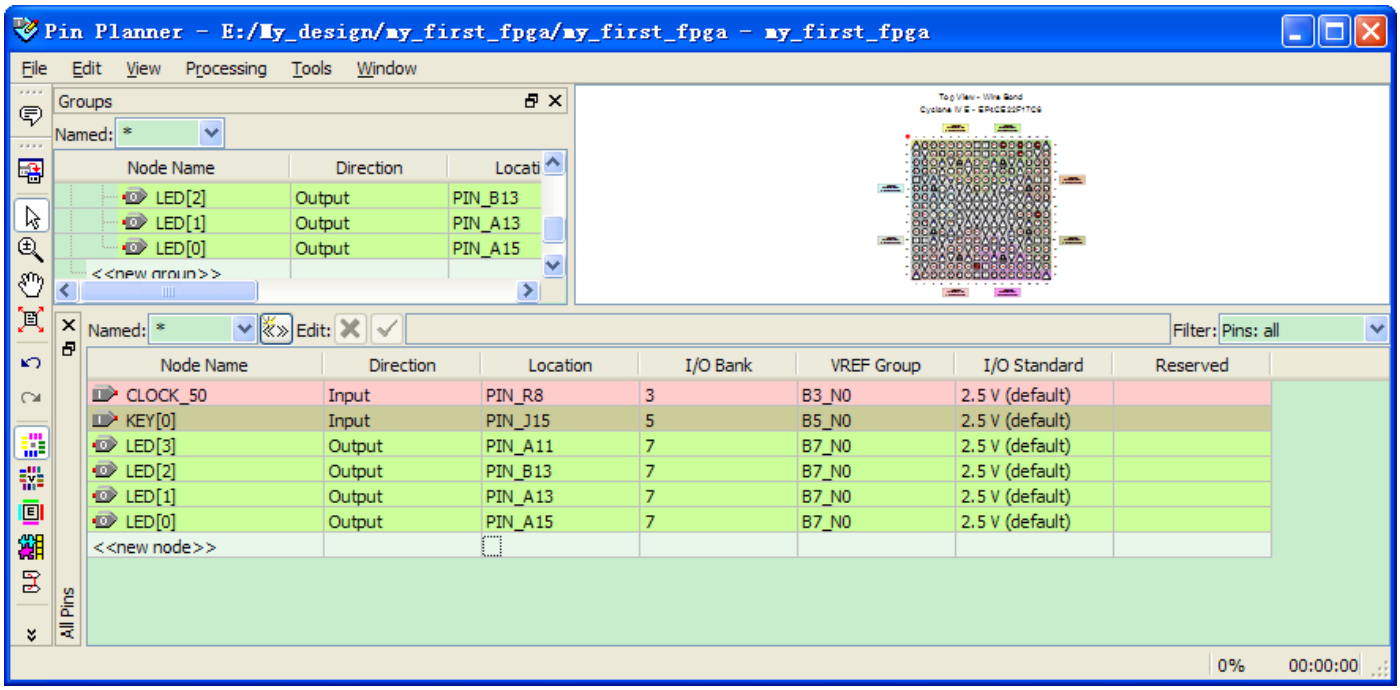
DİP Switch Pinleri

!!!!CLOCK PİNİ:R8

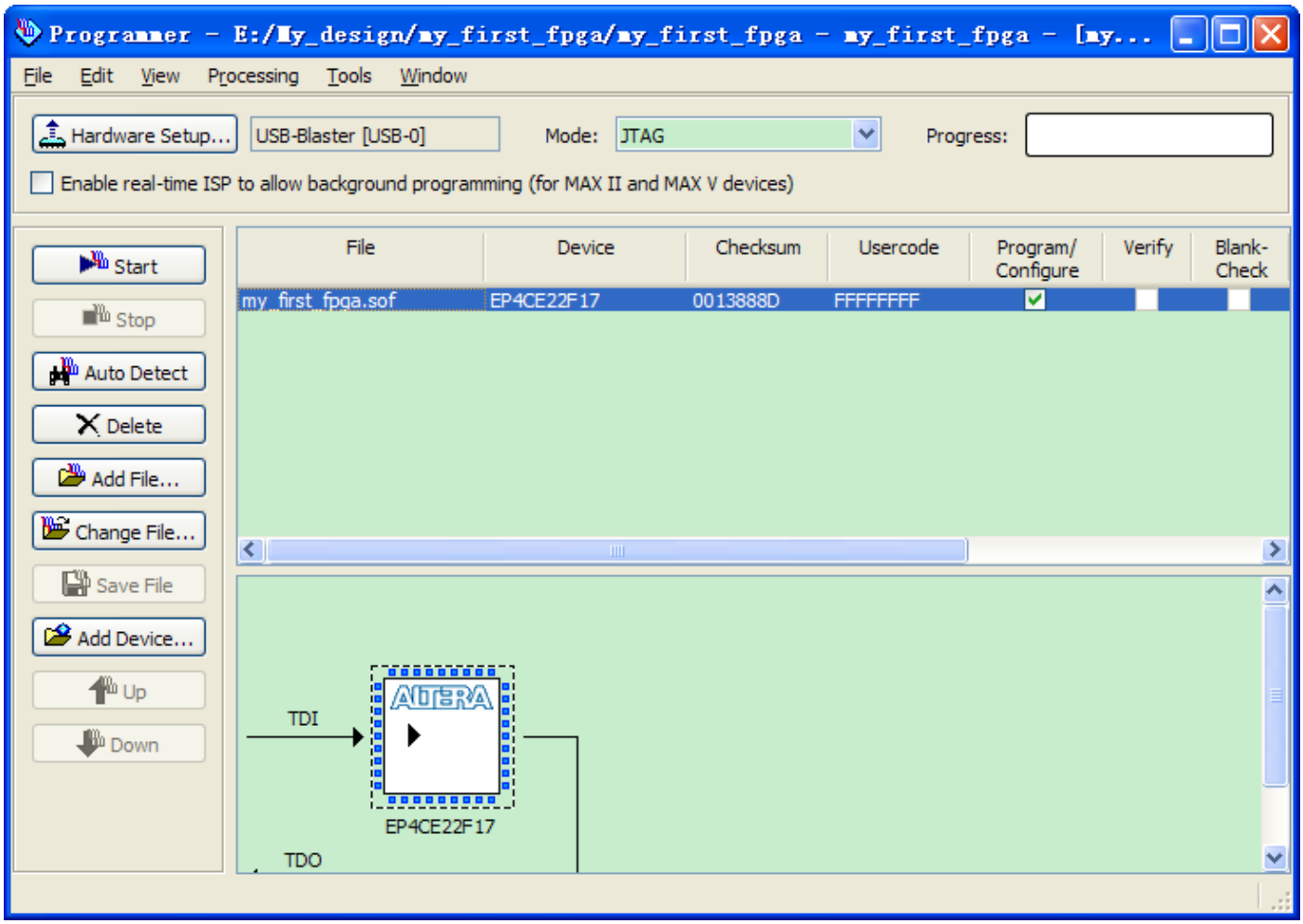
!!NOT:Diğer Pinler için "USER Manuel" bakın…

ÖRNEK UYGULAMA

Pin Name	*FPGA Pin Location*
KEY[0]	J15
LED[3]	A11
LED[2]	B13
LED [1]	A13
LED [0]	A15
CLOCK_50	R8



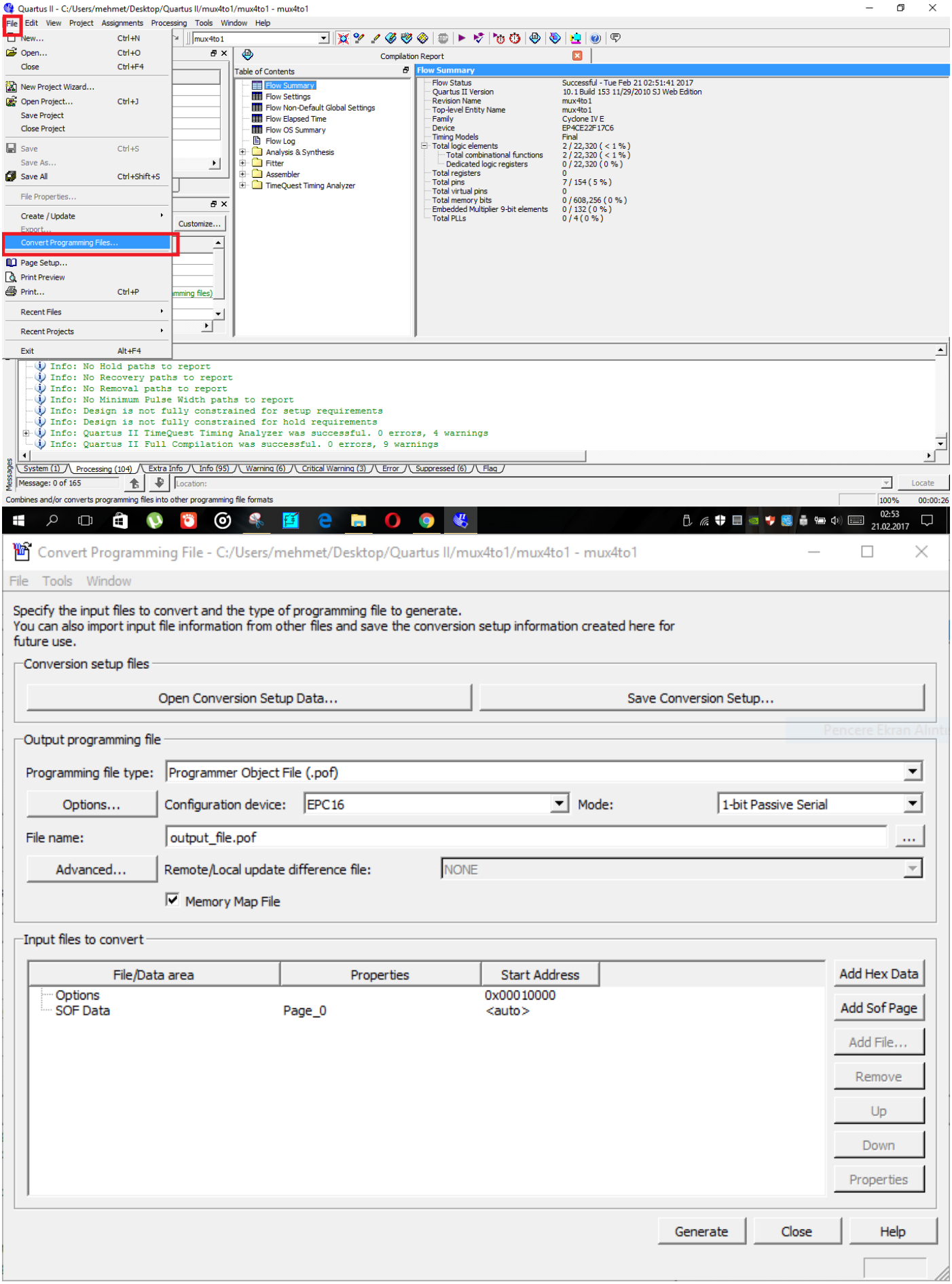
FPGA PROGRAMLAMA:

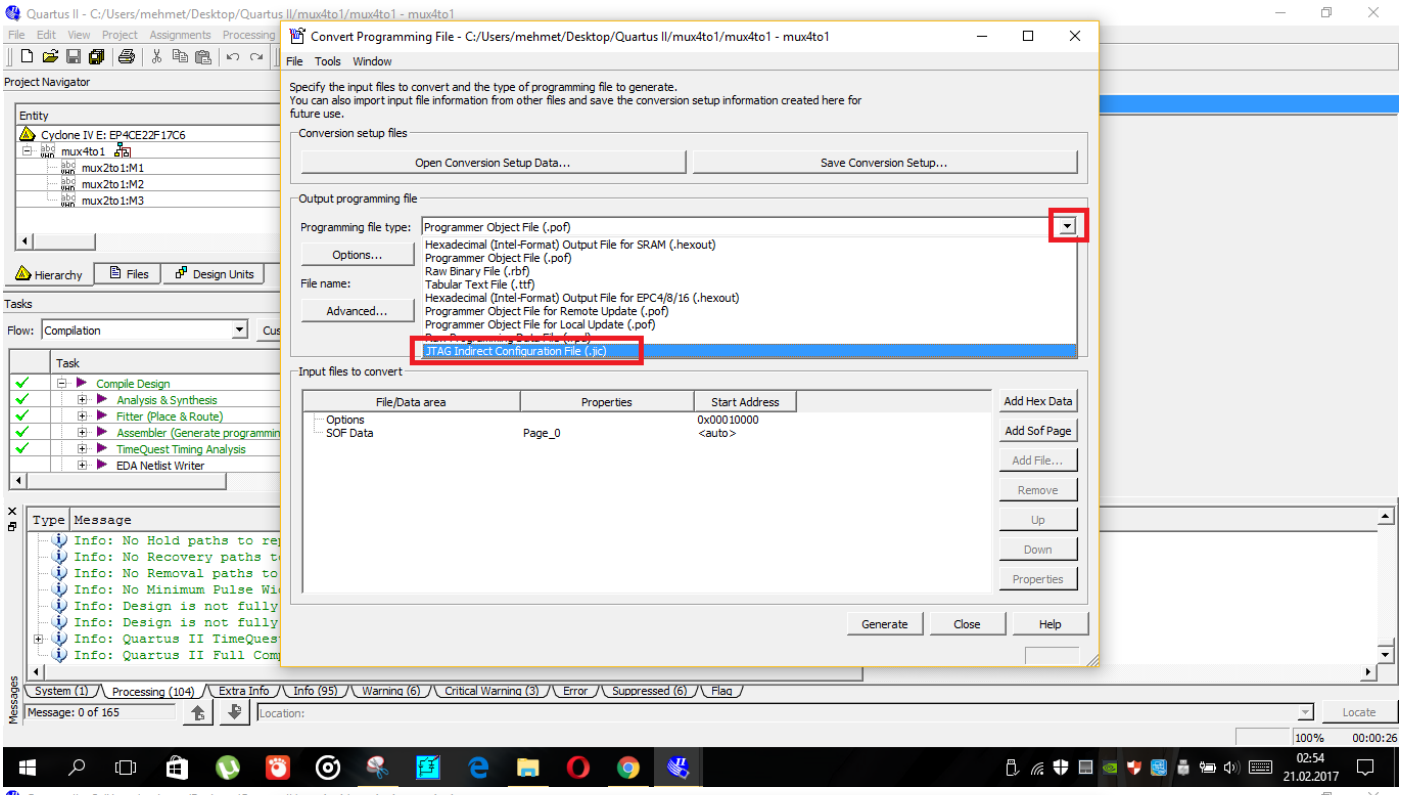


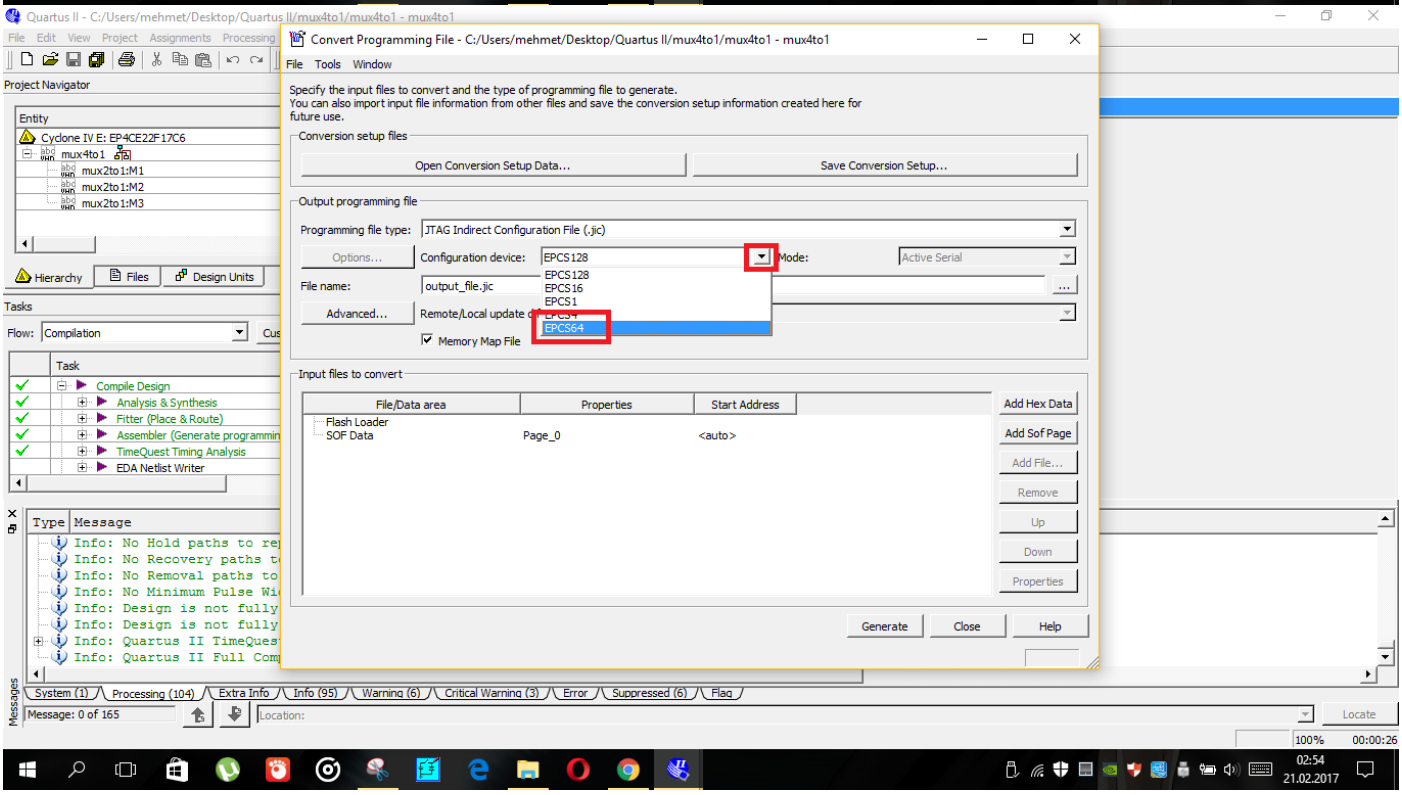
- Program VHDL olarak yazdıktan sonra programı derliyoruz
- Hatalar ve Error mesajlarına bakıp gerekli düzeltmeleri yapıyoruz.
- Pin atamalarını gerçekleştiriyoruz.
- Tüm işlemlerden sonra yukardaki arayüzü kullanarak yazmış olduğumuz programı FPGA'ya yüklüyoruz.

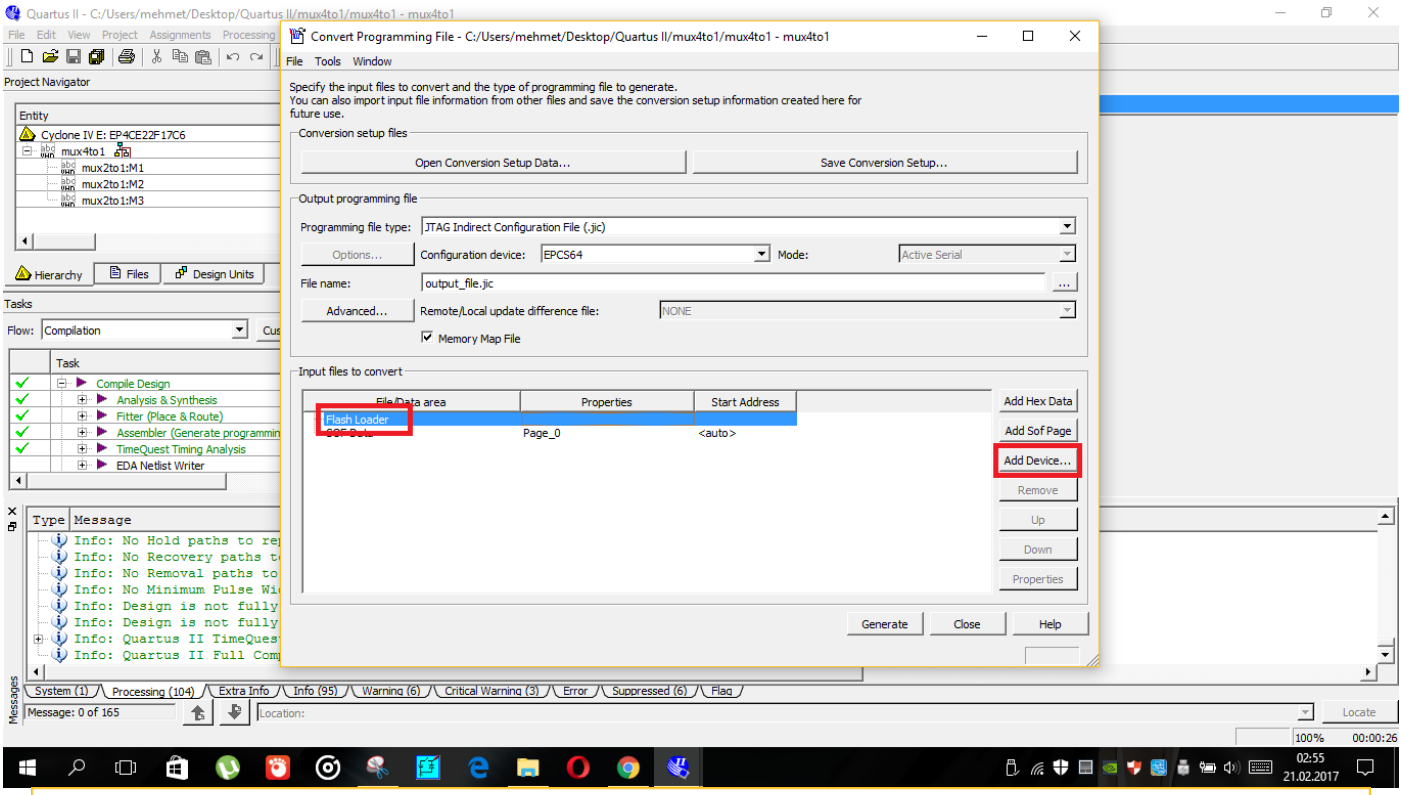
!!!NOT:**""USB-BLASTER""** Yüklenmediği taktirde.Donanımınız **""NO HARDWARE""** Olarak gözükecektir.

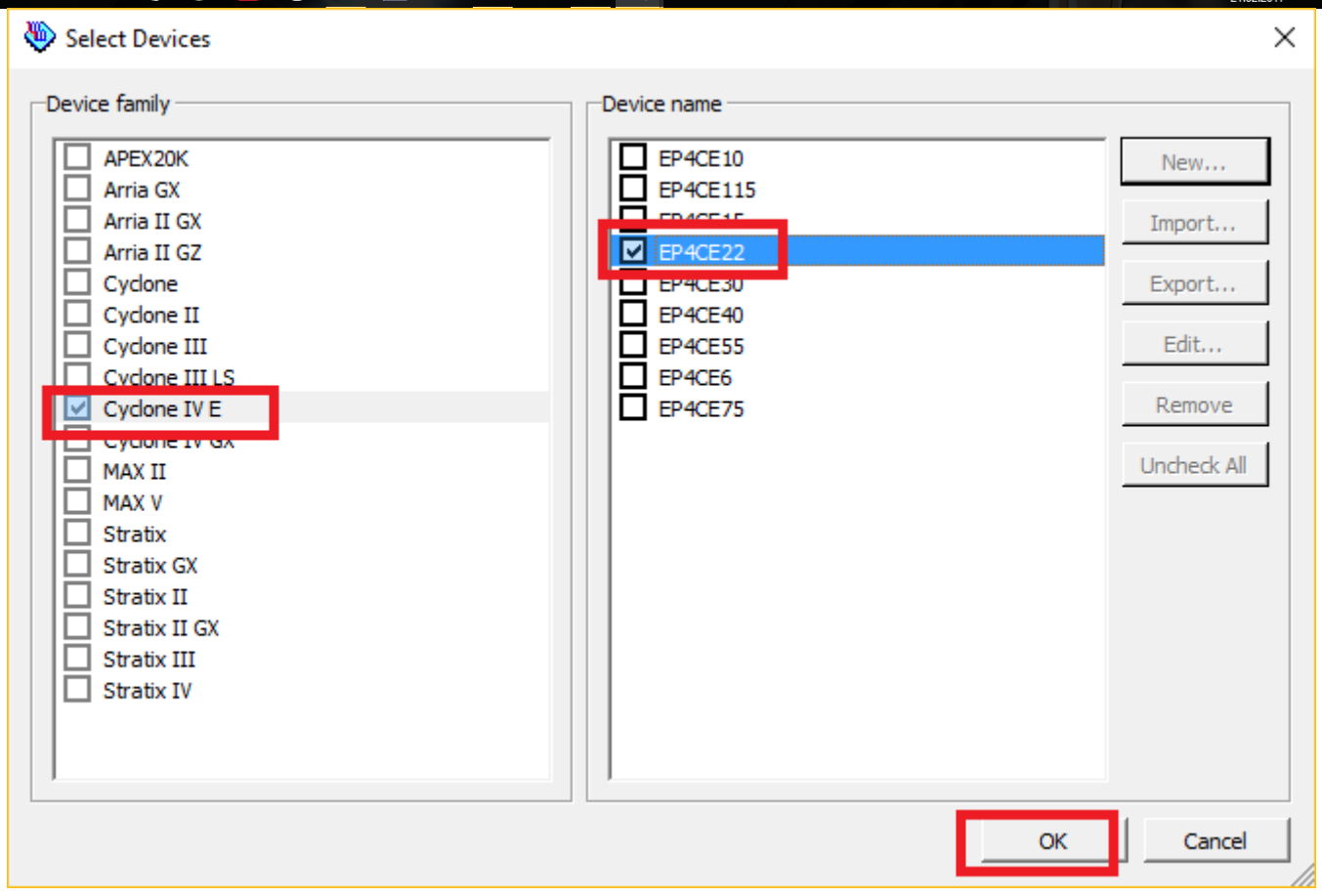
ROM’a Yazma

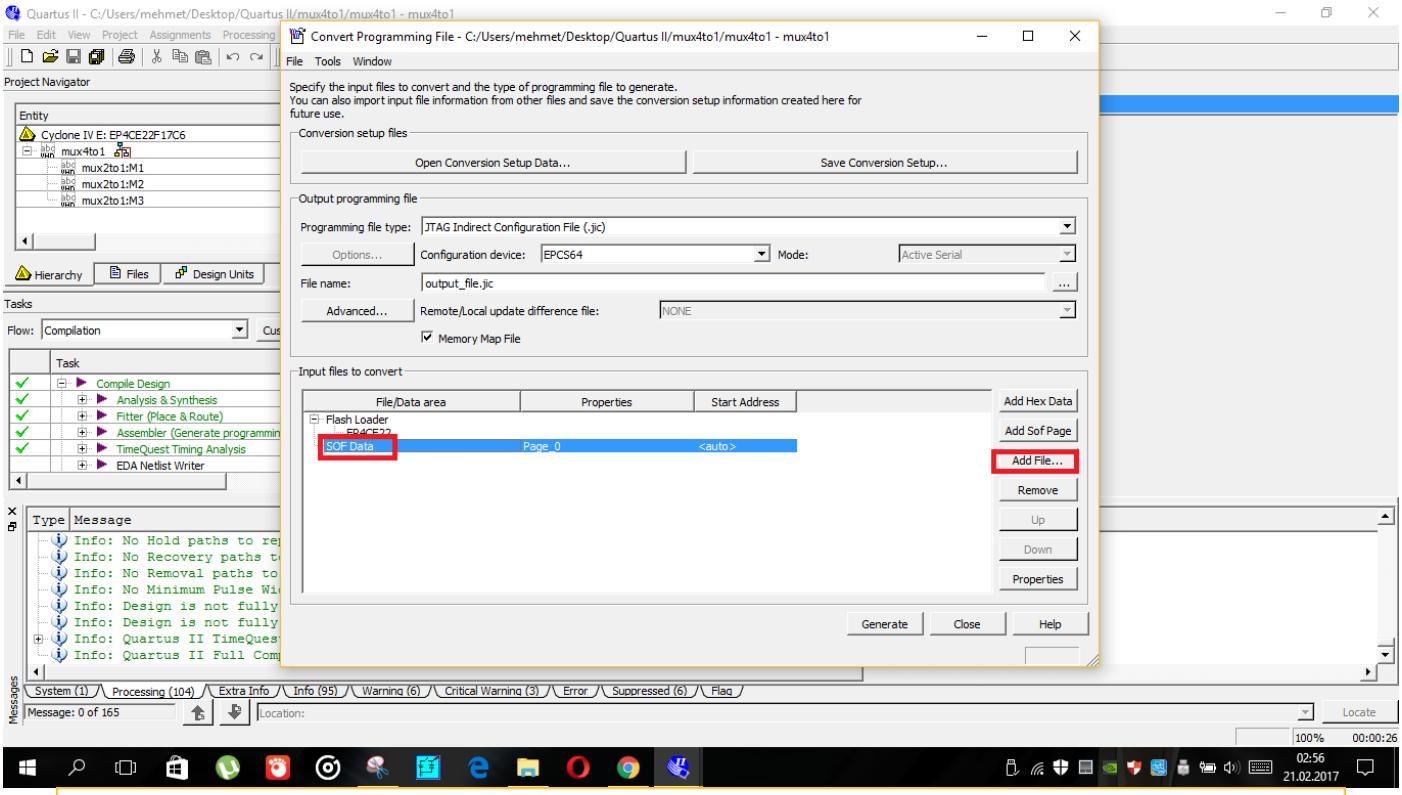

Quartus II - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Edit View Project Assignments Processing Tools Window Help
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
Compilation Report
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
Flow Summary
Flow Status Successful - Tue Feb 21 02:51:41 2017
Quartus II Version 10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name mux4to1
Top-level Entity Name mux4to1
Family Cyclone IV E
Device EP4CE22F17C6
Timing Models Final
Total logic elements 2 / 22,320 (< 1 %)
Total combinational functions 2 / 22,320 (< 1 %)
Dedicated logic registers 0 / 22,320 (0 %)
Total registers 0
Total pins 7 / 154 (5 %)
Total virtual pins 0
Total memory bits 0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements 0 / 132 (0 %)
Total PLLs 0 / 4 (0 %)
Info: No Hold paths to report
Info: No Recovery paths to report
Info: No Removal paths to report
Info: No Minimum Pulse Width paths to report
Info: Design is not fully constrained for setup requirements
Info: Design is not fully constrained for hold requirements
Info: Quartus II TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 9 warnings
System (1) Processing (104) Extra Info Info (95) Warning (6) Critical Warning (3) Error Suppressed (6) Flag
Message: 0 of 165
Location:
Locate
Combines and/or converts programming files into other programming file formats
100%
00:00:26
02:53
21.02.2017
Convert Programming File - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: Programmer Object File (.pof)
Options...
Configuration device: EPC16
Mode: 1-bit Passive Serial
File name: output_file.pof
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Options 0x00010000
SOF Data Page_0 <auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

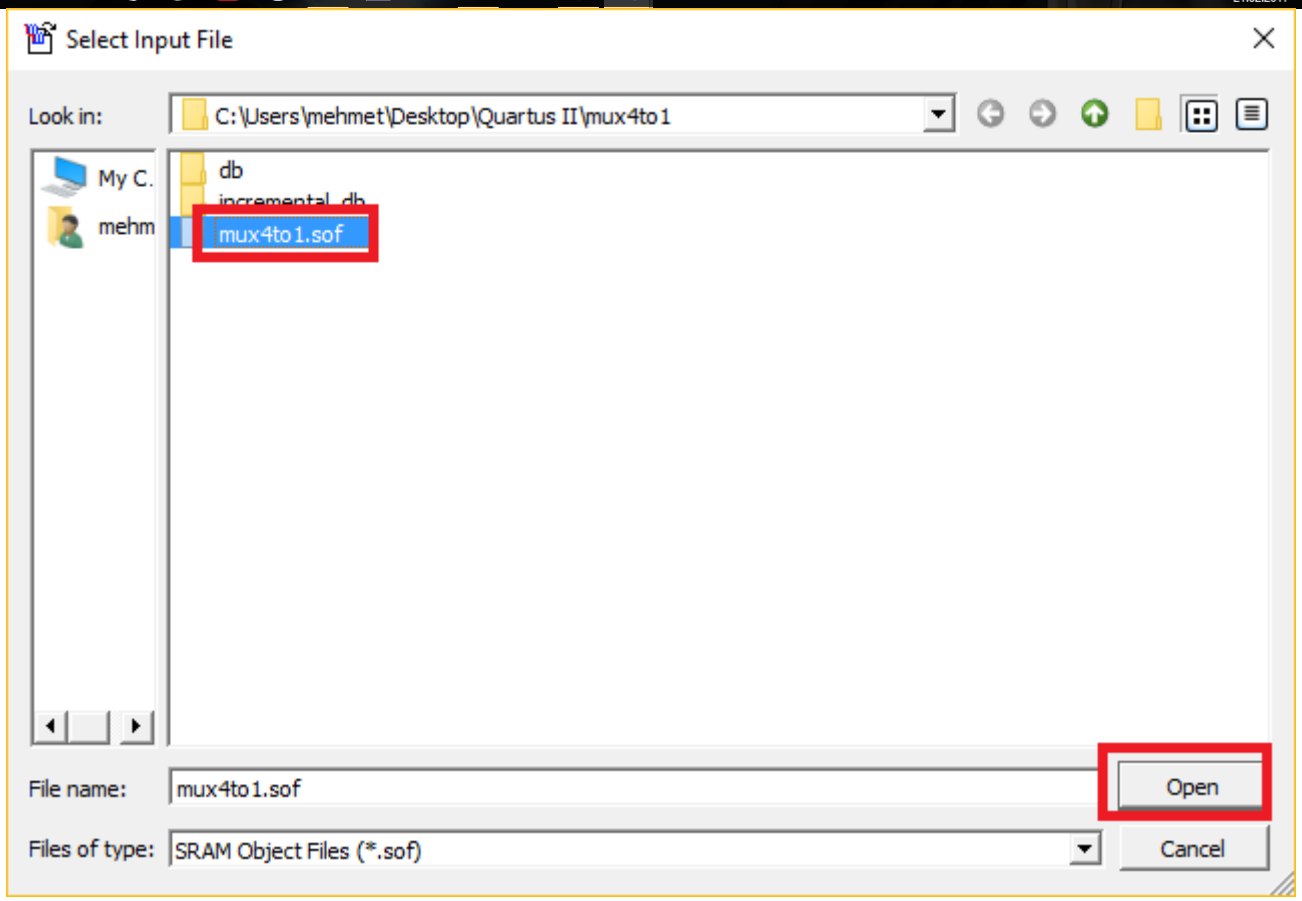

Convert Programming File - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: Programmer Object File (.pof)
Options...
File name:
Advanced...
Hexadecimal (Intel-Format) Output File for SRAM (.hexout)
Programmer Object File (.pof)
Raw Binary File (.rbf)
Tabular Text File (.ttf)
Hexadecimal (Intel-Format) Output File for EPC4/8/16 (.hexout)
Programmer Object File for Remote Update (.pof)
Programmer Object File for Local Update (.pof)
JTAG Indirect Configuration File (.jic)
Input files to convert
File/Data area
Properties
Start Address
Options
0x00010000
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

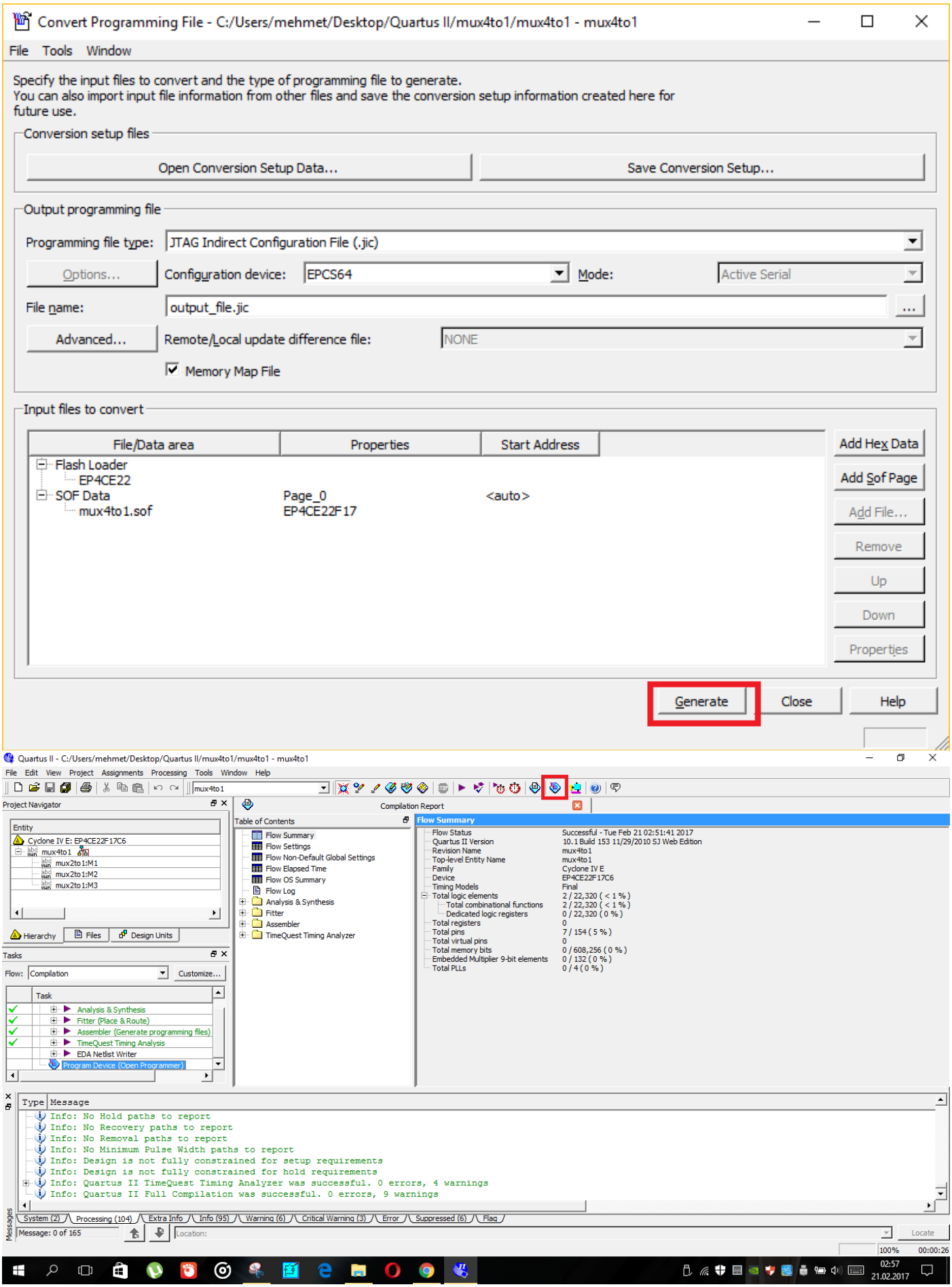

Convert Programming File - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS128
Mode: Active Serial
File name: output_file.jic
Advanced...
Remote/Local update
Memory Map File
EPCS128
EPCS16
EPCS1
EPCS64
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help


Convert Programming File - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS64
Mode: Active Serial
File name: output_file.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
Page_0
<auto>
Add Hex Data
Add Sof Page
Add Device...
Remove
Up
Down
Properties
Generate
Close
Help

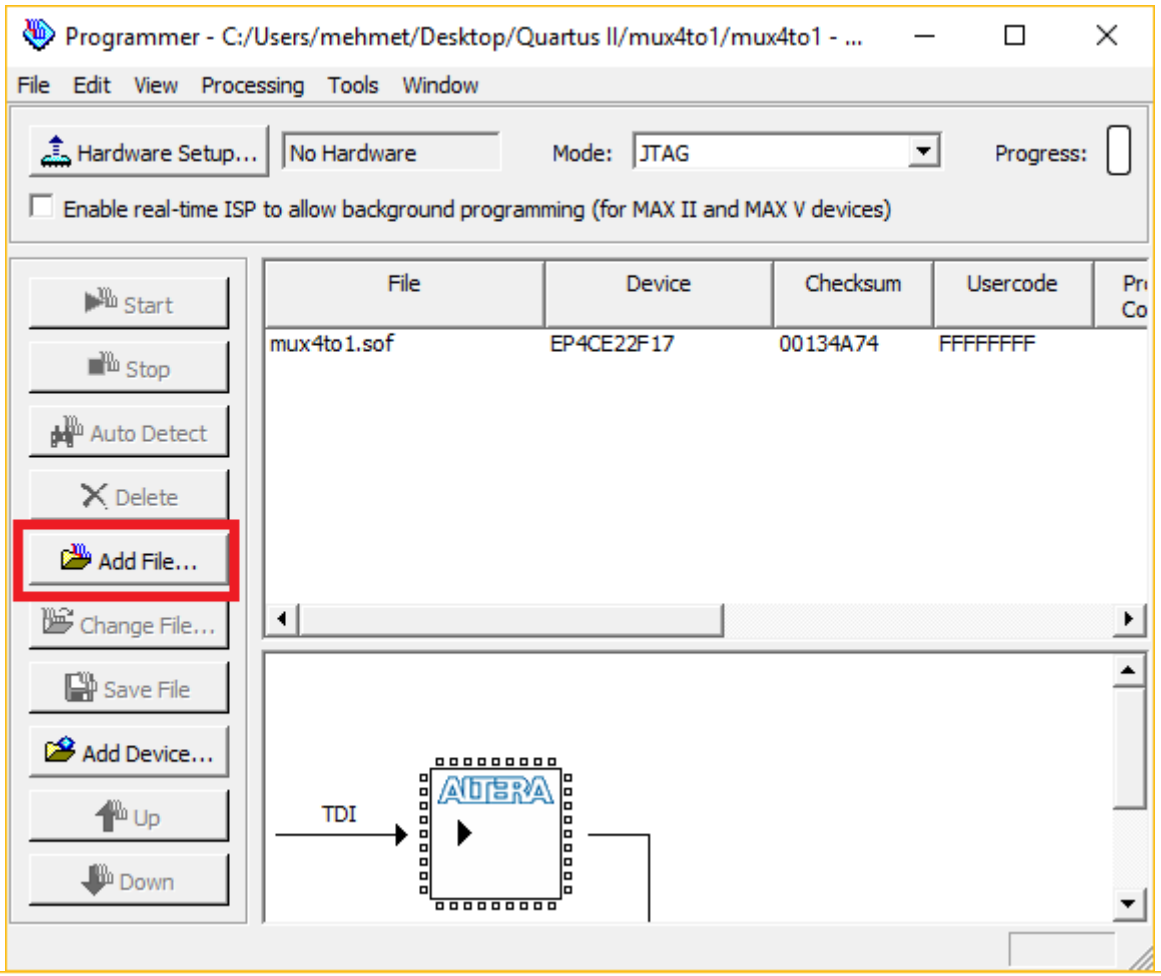

Select Devices
Device family
APEX20K
Arria GX
Arria II GX
Arria II GZ
Cyclone
Cyclone II
Cyclone III
Cyclone III LS
Cyclone IV E
MAX II
MAX V
Stratix
Stratix GX
Stratix II
Stratix II GX
Stratix III
Stratix IV
Device name
EP4CE10
EP4CE115
EP4CE22
EP4CE40
EP4CE55
EP4CE6
EP4CE75
New...
Import...
Export...
Edit...
Remove
Uncheck All
OK
Cancel

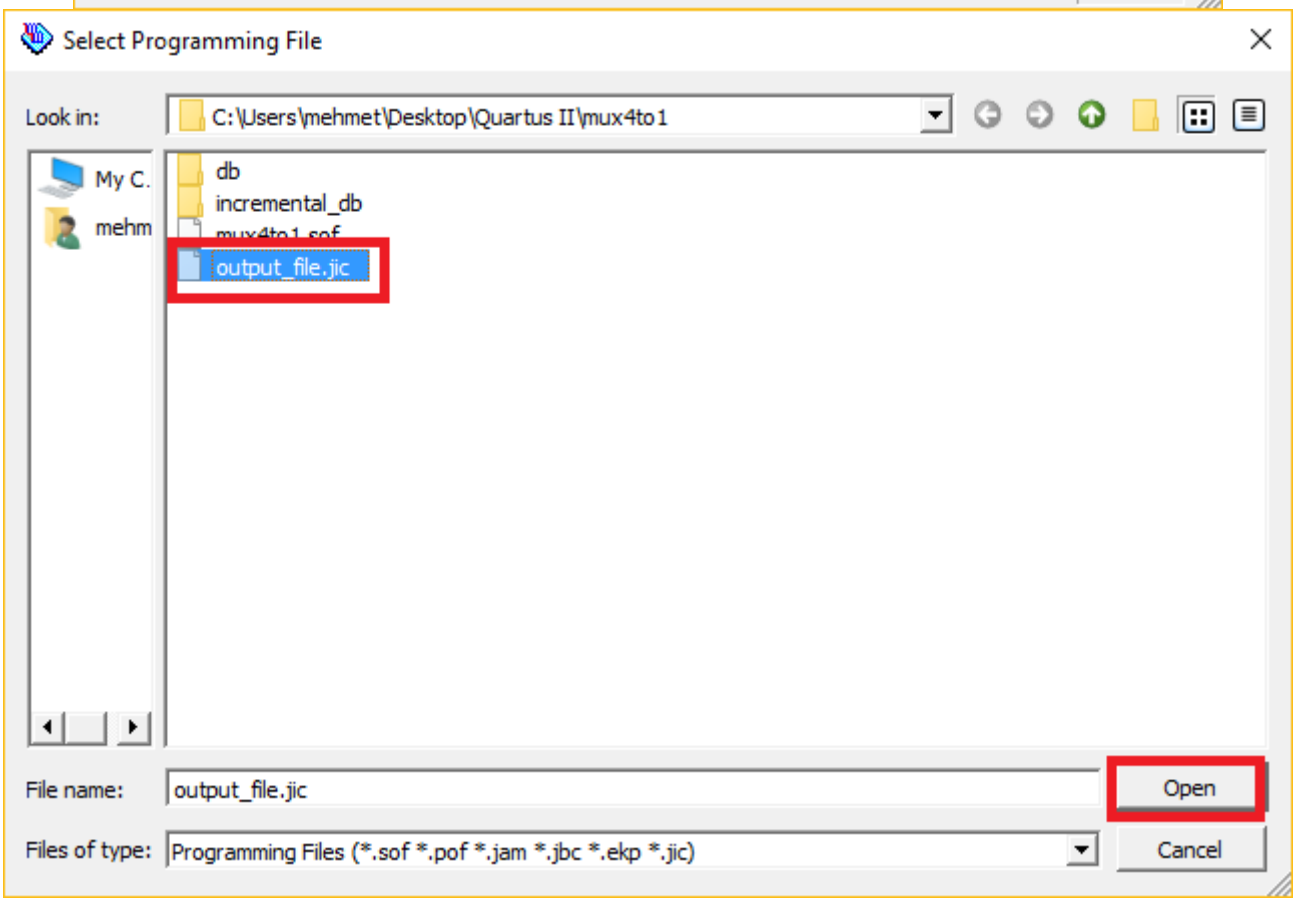

Convert Programming File - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS64
Mode: Active Serial
File name: output_file.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
SOF Data
Page_0
<auto>
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

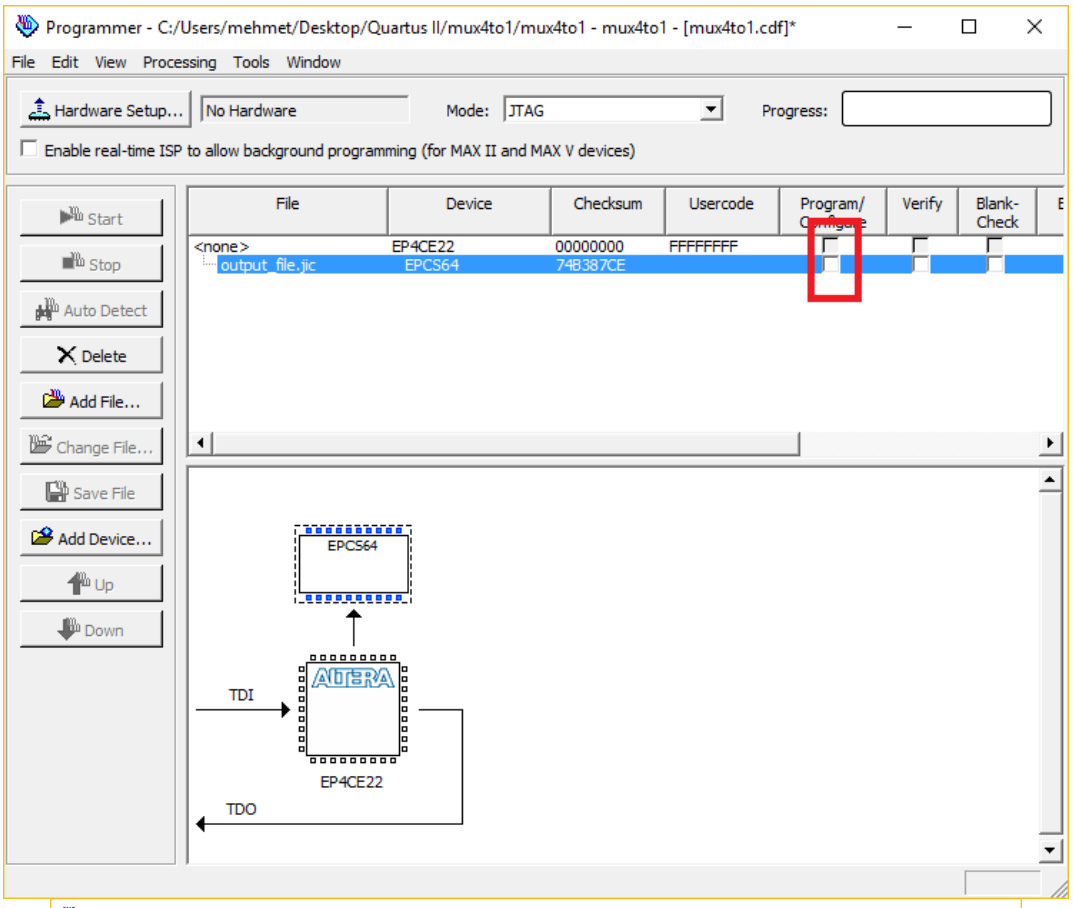

Select Input File
Look in:
C:\Users\mehmet\Desktop\Quartus II\mux4to1
db
mux4to1.sof
File name:
mux4to1.sof
Open
Files of type:
SRAM Object Files (*.sof)
Cancel

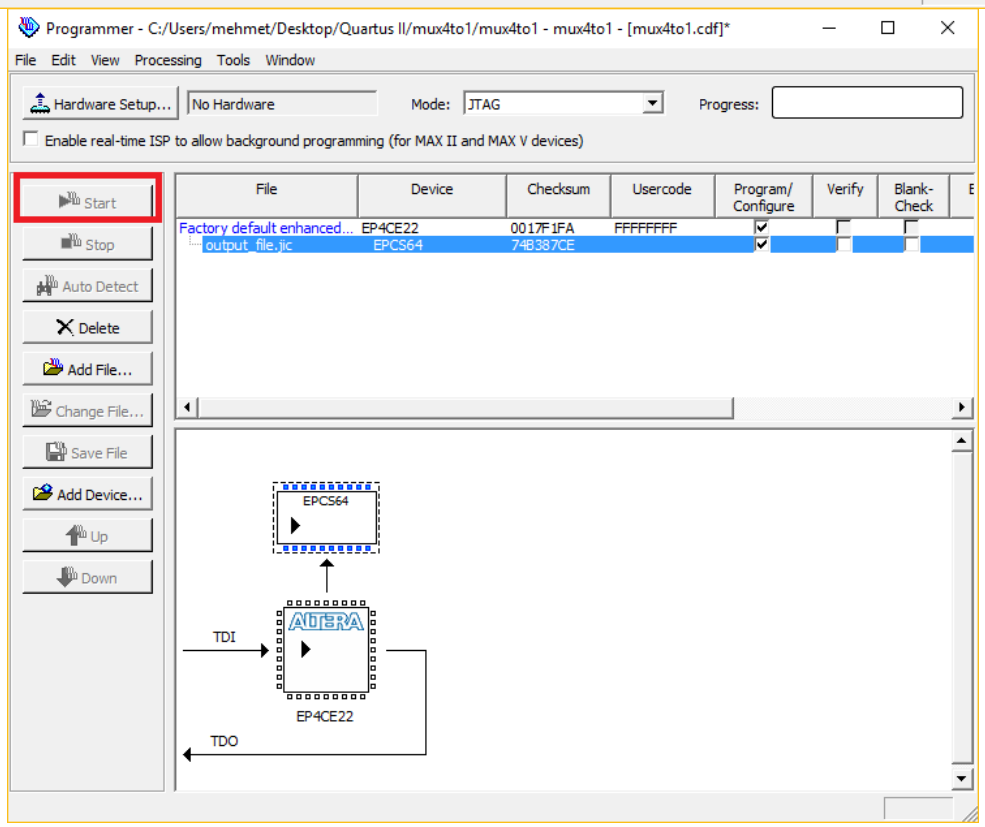

Convert Programming File - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Tools Window
Specify the input files to convert and the type of programming file to generate.
You can also import input file information from other files and save the conversion setup information created here for future use.
Conversion setup files
Open Conversion Setup Data...
Save Conversion Setup...
Output programming file
Programming file type: JTAG Indirect Configuration File (.jic)
Options...
Configuration device: EPCS64
Mode: Active Serial
File name: output_file.jic
Advanced...
Remote/Local update difference file: NONE
Memory Map File
Input files to convert
File/Data area
Properties
Start Address
Flash Loader
EP4CE22
SOF Data
Page_0
<auto>
mux4to1.sof
EP4CE22F17
Add Hex Data
Add Sof Page
Add File...
Remove
Up
Down
Properties
Generate
Close
Help

Quartus II - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Entity
Cyclone IV E: EP4CE22F17C6
mux4to1
mux2to1:M1
mux2to1:M2
mux2to1:M3
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
Compilation Report
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
Flow Summary
Flow Status Successful - Tue Feb 21 02:51:41 2017
Quartus II Version 10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name mux4to1
Top-level Entity Name mux4to1
Family Cyclone IV E
Device EP4CE22F17C6
Timing Models Final
Total logic elements 2 / 22,320 (< 1 %)
Total combinational functions 2 / 22,320 (< 1 %)
Dedicated logic registers 0 / 22,320 (0 %)
Total registers 0
Total pins 7 / 154 (5 %)
Total virtual pins 0
Total memory bits 0 / 608,256 (0 %)
Embedded Multiplier 9-bit elements 0 / 132 (0 %)
Total PLLs 0 / 4 (0 %)
Type Message
Info: No Hold paths to report
Info: No Recovery paths to report
Info: No Removal paths to report
Info: No Minimum Pulse Width paths to report
Info: Design is not fully constrained for setup requirements
Info: Design is not fully constrained for hold requirements
Info: Quartus II TimeQuest Timing Analyzer was successful. 0 errors, 4 warnings
Info: Quartus II Full Compilation was successful. 0 errors, 9 warnings
System (2) Processing (104) Extra Info Info (95) Warning (6) Critical Warning (3) Error Suppressed (6) Flag
Message: 0 of 165
Location:
Locate
100%
00:00:26
02:57
21.02.2017


Programmer - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - ...
File Edit View Processing Tools Window
Hardware Setup...
No Hardware
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
mux4to1.sof
EP4CE22F17
00134A74
FFFFFFFF
TDI


Select Programming File
Look in:
C:\Users\mehmet\Desktop\Quartus II\mux4to1
My C.
mehm
db
incremental_db
output_file.jic
File name:
output_file.jic
Open
Files of type:
Programming Files (*.sof *.pof *.jam *.jbc *.ekp *.jic)
Cancel


Programmer - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1 - [mux4to1.cdf]*
File Edit View Processing Tools Window
Hardware Setup...
No Hardware
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
<none>
EP4CE22
00000000
FFFFFFFF
output_file.jic
EPCS64
74B387CE
EPCS64
TDI
EP4CE22
TDO


Programmer - C:/Users/mehmet/Desktop/Quartus II/mux4to1/mux4to1 - mux4to1 - [mux4to1.cdf]*
File Edit View Processing Tools Window
Hardware Setup...
No Hardware
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
Factory default enhanced...
EP4CE22
0017F1FA
FFFFFFFF
output_file.jic
EPCS64
74B387CE
EPCS64
TDI
EP4CE22
TDO